UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,624	10/28/2003	Ryan Taylor Herbst	5693P225	5633

48102 7590 10/26/2006

NETWORK APPLIANCE/BLAKELY
12400 WILSHIRE BLVD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 10/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,624	HERBST ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *18-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed August 8, 2006 in response to PTO Office Action dated May 11, 2006. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-17 have been presented for examination in this application.

Please note the change in Examiner attributed to the current application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daynes (US# 6,343,339) and Tanenbaum.

Regarding claim 1, Daynes teaches a processor [proc. (113)] for offloading processing in a storage environment, comprising: a processor interface [Comm. Int. (120)] that interfaces said processor to a network processor [server (126)] configured to

perform a storage function; and semaphore [circuitry], coupled to said processor interface, that receives a signal from said network processor, and that controls a semaphore related to said signal for locking and unlocking access to data [proc. receives messages/code [col. 6, lines 50-52 & 58-59], which may be OOP [col. 7, lines 17-34], which extends to locking/unlocking operations [col. 8, lines 11-29]; see also column 11, lines 7-33; col. 6, lines 35-40 & 50-56].

However, Daynes fails to teach that the semaphore comprises hardware circuitry. Tanenbaum teaches that hardware and software are logically equivalent [page 11].

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Daynes and Tanenbaum before him at the time the invention was made to modify the semaphore software of Daynes to include that of the hardware, as taught by Tanenbaum, in order to realize benefits in cost, speed, and reliability [page 11, para. 3].

Regarding claim 2, Daynes teaches, wherein said semaphore circuitry manages a queue for access to said semaphore [queue, col. 11, lines 20-22].

Regarding claim 3, Daynes teaches wherein said semaphore circuitry receives a second signal from said network processor and removes a request from said queue in response to said second signal when said network processor no longer desires said semaphore [clearing deadlock conflict].

Regarding claim 4, Daynes teaches wherein said semaphore circuitry refrains from sending to said network processor a second signal indicating said semaphore is unavailable, whereby said network processor continues to wait for said semaphore and said semaphore circuitry maintains ordered access to said queue [col. 11, lines 28-29].

Regarding claim 5, Daynes teaches that said signal comprises one of a plurality of access requests for one of a plurality of semaphores, wherein said semaphore circuitry manages said plurality of access requests in a plurality of queues, and wherein each of said plurality of queues corresponds to a respective one of said .plurality of semaphores [TILS (column 15, line 40)].

Regarding claim 6, Daynes teaches a command queue that stores said signal received from said network processor [wait queue].

Regarding claims 7-8, and 10, Daynes teaches that said semaphore is a structure in a hash array, and wherein said semaphore circuitry comprises a hash key generator that performs a hashing function on said signal for accessing said hash array; an update engine that receives a second signal from said network processor relating to a first process thread on said network processor, releases a lock on said semaphore related to said second signal, and sends a third signal to said network processor associating said semaphore with a second process thread on said network processor

[TILS can be implemented as a hash table (column 15, line 43); locking and releasing the lock and acknowledgment that the lock is available].

As per claim 9, Daynes discloses a semaphore queue manager that manages a queue of a plurality of semaphores [lock manager].

As per claims 11-17, claims 11-17 encompass the same scope of the invention as those of claims 1-10. Therefore, claims 11-17 are rejected for the same reasons as stated above with respect to claims 1-10.

Claims 1 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (Applicant's Admitted Prior Art) and Tanenbaum.

As per claim 1, AAPA discloses a processor [host 12] for offloading processing in a storage environment, comprising: a processor interface [network 14] that interfaces said processor to a network processor configured to perform a storage function [storage server 16]; and semaphore [circuitry],coupled to said processor interface, that receives a signal from said network processor, and that controls a semaphore related to said signal for locking and unlocking access to data [controlling access to data space by semaphore management for individual process threads; prohibits other threads from accessing space currently accessed by original thread; performed within server (16); para 0009 & 0010].

However, AAPA fails to teach that the semaphore comprises hardware circuitry. Tanenbaum teaches that hardware and software are logically equivalent [page 11]. Therefore it would have been obvious to one of ordinary skill in the art having the teachings of AAPA and Tanenbaum before him at the time the invention was made to modify the semaphore software of AAPA to include that of the hardware, as taught by Tanenbaum, in order to realize benefits in cost, speed, and reliability [page 11, para. 3].

Regarding claim 11, AAPA teaches a method of controlling a processor [host (12)] for offloading processing in a storage environment, comprising the steps of: receiving a signal from a network processor configured to perform a storage function; controlling a semaphore [not req. to be hardware; para 0010] related to said signal for locking and unlocking access to data [controlling access to data space by semaphore management for individual process threads; prohibits other threads from accessing space currently accessed by original thread; performed within server (16); para 0009 & 0010].

Response to Arguments

Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to

4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Primary Examiner
Art Unit 2187
October 23, 2006